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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/426,991	10/26/1999	TATSUYA TAKAHASHI	2933SE-85	2606

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SHERIDAN ROSS PC
1560 BROADWAY
SUITE 1200
DENVER, CO 80202

EXAMINER
YE, LIN

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/426,991	AKAHASHI, TATSUYA
	Examiner	Art Unit
	Lin Ye	2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings 6A and 6B are objected to because:

The label " From **flame** transfer completion..." should be corrected to -- From **frame** transfer completion...--.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe et al. U.S. Patent 6,351,284.

Referring to claim 1, the Watanabe reference discloses in Figures 1-5, a methos for driving a solid state image sensor that provides image signals in display image units, wherein the solid state image sensor (10) includes a semiconductor substrate (11), a semiconductor layer formed on the semiconductor substrate and having an opposite conductivity to the

semiconductor substrate, the semiconductor layer having a plurality of parallel channel regions (12 & 13) arranged therein, and a plurality of transfer electrodes (15 & 16) arranged on the semiconductor substrate each intersecting the plurality of channel regions, wherein each of the channel regions generates and accumulates information charges (See Col. 1, lines 36-53), the driving method comprising the steps of (See Figure 2): storing information charges in the channel region that correspond to a transfer electrode selected by selectively activating the plurality of transfer electrodes at a predetermined timing during a vertical scanning period (See Col. 2, lines 16-21); transferring the stored information charges to a transfer register (the horizontal transfer section 1h is comprised of a shift register, See Col. 5, lines 20-25); discharging the information charges in the channel regions toward the semiconductor substrate by keeping the plurality of transfer electrodes deactivated and increasing the potential at the semiconductor substrate as shown in Figure 2 (See Col. 26-37); repetitively executing the storing, transferring, and discharging steps to continuously obtain the image signals in display image (reproducing image) units.

Referring to claim 2, the Watanabe reference discloses wherein the potential at the semiconductor substrate is raised just before the next storing step (when discharging information charges stored in the pixels, the potential at the semiconductor substrate is raised. The next storing information charges period indicated by a period L is started after the discharging complete immediately as shown in Figure 2).

Referring to claim 3, the Watanabe reference discloses wherein a potential well (depletion layer is formed in the channel region 17 in the buried layer 13) having a

predetermined depth is formed in the selected channel region during the storing step to store the information charges as shown in Figure 3.

Referring to claim 4, the Watanabe reference discloses wherein the potential well is prevented from being formed in the discharging step (See Col.2, lines 19-24).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. U.S. Patent 6,351,284 in view of Yadokoro et al. Japan Publication 09-168118.

Referring to claim 5, the Watanabe reference discloses all subject matter as discussed in respected claim 1, except the reference does not explicitly show the system deactivates the vertical clock signal so that the transfer electrodes are maintained in a deactivation state after transferring the stored information charges.

The Yadokoro reference discloses in Figures 1 and 4-5, a solid-state camera including a pulse-control circuit (7). When a signal charge is read (after transferring the stored information charges), it deactivates the vertical clock signal (ϕ v) and horizontal clock signal and reset signal (See page 3, [0019]). The Yadokoro reference is an evidence that one of ordinary skill in the art at the time to see more advantages for deactivating the vertical clock

signal after transferring the stored information charges, because it can suppress the excessive heat generation due to the useless drive of the registers and a charge detector and the dark current is reduced and the S/N is improved. For those reasons, it would have been obvious to see the system deactivates the vertical clock signal so that the transfer electrodes are maintained in a deactivation state after transferring the stored information charges by Watanabe.

Referring to claim 6, the Watanabe reference discloses wherein the clock generator activates the substrate clock signal (discharging signal ϕ b or shutter operation) to raise the potential at the semiconductor substrate except when the information charges are stored (during the period L as shown in Figure 2).

Referring to claim 7, the Yadokoro reference discloses wherein the clock generator (a pulse generator 6) keeps the substrate clock signal (reset pulse ϕ R) deactivated to keep the plurality of transfer electrodes deactivated (vertical clock signal ϕV deactivated when a signal charge is read) except when the information charges are stored (accumulated).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Lin Ye
June 25, 2003